REMARKS

Claims 1-12, 13, and 15-23 are pending in this application. Claim 13 is amended, and claim 14 is cancelled without prejudice or disclaimer. Claims 1-12 have been allowed. Claims 13 and 15-23 have been rejected. For the following reasons, this application stands in a condition for allowance.

In response to our arguments filed on August 30, 2002, the Examiner withdrew the anticipation rejection of claims 13 -15 citing Otsuka and withdrew the anticipation rejection of claims 16-17 citing Lee, but rejects pending claims 13-23 on new grounds. Specifically, the Examiner rejects claims 13-14 and 18-19 under 35 U.S.C. §102(e) as being anticipated by Egawa (U.S. Patent No. 6,289,481); rejects claims 15, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Otsuka in view of Egawa; and rejects claims 16, 17, 22, and 23 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Toda. The rejections are respectfully traversed.

Rejection of claims 13, 14, 18, and 19 under 35 U.S.C. §102(e) (Egawa)

Egawa discloses circuitry to shorten data read times by performing error correction on low order and high order of bits at different times. Referring to the prior art illustrated by Fig. 1 of Egawa, an ECC circuit 6 performs error correcting on both low and high digit data output by *conversion circuit 3*. Access time is somewhat delayed by the time it takes to detect multi-level voltage values stored by the memory cell and to convert those values to two-bit data, which is output by a conversion circuit. Referring to the corresponding timing diagram of Figure 5, latch control signal P is not activated until both low digit data and high digit data are input at time t11. Time between acquiring low

digit data and high digit data also contributes to the delay. In order to increase access time (Fig. 6), Egawa provides respective ECC circuits 61 and 62 for performing error correction of low digit data and high digit data, respectively. Thus, referring to the corresponding timing diagram of Figure 9, lower digit data is latched at time t4, whereas higher digit data is output at time t5 and is latched at a later time, t8, thus increasing access time.

Also, in the Egawa reference, data readout operation is relatively delayed because the data is output only after the word line selection operations are performed three times and DATA1-DATA3 are read out from binary conversion circuit 3. Specifically, the potential level of the word line is sequentially driven to Vg1, Vg2, and Vg3, respectively (see Figs. 7A and 7B, col. 5, line 47 - col. 6, line 29). Lower Digit Data is determined by DATA2, *i.e.*, read when the potential of the word line is Vg2. Higher Digit Data is determined by DATA 1 and DATA3 that are read when the potential of the word line is Vg1 and Vg3, respectively. The read data is stored in binary conversion circuit 3, and then are output from the circuit at the timing in accordance with Fig. 9. Thus, in Egawa, Higher Digit Data can be determined only after DATA1-DATA3 are read out from binary conversion circuit 3, which means that the data can be output only after the word line selection operation is performed three times.

The subject matter of claim 14 has been incorporated in claim 13, and claim 13 now recites that "said step of outputting said part of said plurality of data overlaps with said step of reading another part of said plurality of data." Also, claim 13 now recites that the "non-volatile semiconductor memory device include[es]...a read circuit reading said data by selecting a word line connected to said memory cell" and that the steps of

reading a part and another part of said plurality of data from said memory cell is accomplished at least in part "by selecting said word line" in each step.

There is no disclosure of reading low digit data and high digit data from a memory cell "by selecting said word line" and that these steps overlap, as claim 13 now recites. Instead, Egawa provides respective ECC circuits 61 and 62 for performing error correction of low digit data and high digit data, respectively, which are *output by binary conversion circuits 3*.

The Examiner alleges that the claimed "reading another part of said plurality of data" and "outputting said another part of said plurality of data" correspond to the operation between time t5 and t8, and that the reading steps overlap after time t5. This is not the case.

The Examiner assumes that, because the representative levels of each signal of the timing diagram (Fig. 9) change at a designated time (t1, t2, t3, etc.) and remain at the new level seemingly indefinitely, the reading steps overlap. To the contrary, Egawa teaches (col. 6, lines 30-44) that lower digit data is output from binary conversion circuit 3 at time t2 and latching of lower digit data is completed at time t4. After that time, time t5, higher digit data is output and is latched at time t8. Thus, the output of data by binary conversion circuit 3 is sequential, and are not overlapping by any means. Accordingly, Egawa does not teach "outputting said part of said plurality of data overlaps with said step of reading another part of said plurality of data," as claim 13 now recites.

Also, as in claim 13, reading data from the memory cell (the selection of the word line) overlaps with the output of data to an output node. In Egawa, Lower Digit Data and

Higher Digit Data are complied first by binary conversion circuit 3 before outputting binary data to an output node, *i.e.*, prior to time t1.

For the foregoing reasons, Egawa fails to anticipate amended claim 13. Claims 18 and 19 are patentable at least based on dependency therefrom. Withdrawal of the rejection is respectfully solicited.

Rejection of claims 15, 20, and 21 under 35 U.S.C §103(a) (Otsuka in view of Egawa)

Claim 15 recites, *inter alia*, "reading first data from said first memory cell with selectively activating said word line; outputting said first data to said data output node; reading second data from said second memory cell with selectively activating said word line; and outputting said second data to said data output node, wherein said step of outputting said first data overlaps with said step of reading second data." (*emphasis added*).

The Examiner acknowledges that Otsuka does not specifically teach the first and second memory cells coupled to the same word line, and therefore, does not teach that the step of outputting data overlaps with the step of reading data. The Examiner, however, relies on the teachings of Egawa discussed above. The Examiner states:

> It would have been obvious to use the same word line for reading first and second data and provide the step of outputting data overlaps with step of reading data in Otsuka's memory device, because this pipeline or parallel method would reduce the memory access time and speed of the data transfer, therefore, the whole system is enhanced and more efficient."

The Examiner's interpretation of the references and stated motivation to combine is flawed. In the conventional DRAM disclosed by Otsuka, the step of outputting a part of data never overlaps with the step of reading another part of data. Egawa is also deficient in this regard, as discussed above. Specifically, Egawa does not teach reading

data from memory cells, but instead from binary conversion circuits 3. Nevertheless, there is no suggestion of data read from memory cell 5 in steps that overlap one another, as claim 13 recites. Instead, data is sequentially read from cell 5.

Assuming *arguendo*, if the reference were combined, the proposed modification would not render an enhanced and more efficient device, as the Examiner suggests. For instance, Egawa teaches increasing access time when performing ECC on multi-level digit data output by a binary conversion circuit 3. Otsuka teaches a conventional DRAM having a sense amplifier 14 that sequentially outputs data on respective data lines DL1 or DL2 to bus exchanger 16. Otsuka, however, is not concerned with ECC, but rather reading data with a double-data rate (DDR) mode. By incorporating the teaching of Egawa, it is not clear how the combination would render a more efficient device, especially as Egawa relates to ECC whereas Otsuka relates to DDR mode processing. The Examiner has failed to establish a prima facie case of obviousness.

For the foregoing reasons, the combination of Egawa and Otsuka fail to teach the element of claim 15. Claims 20 and 21 are patentable at least based on dependency therefrom. Withdrawal of the rejection is respectfully solicited.

Rejection of claims 16-17 and 22-23 under 35 U.S.C. §103(a) (Lee in view of Toda)

From the previous response, the Examiner withdrew the anticipation rejection, and in response, acknowledged that Lee fails to disclose or suggest writing data from different registers into a single memory cell. Specifically, Lee addresses problems attendant time requirements for programming and verifying data chunks in EEPROM, which far exceed time requirements for providing address and data for each chunk of data. Lee provides that that chucks of data are sequentially latched into first - fourth

registers in response to latch enable signals and concurrently written into the respective subarrays. As there is only one row decoder per sub-array, only one memory cell can be selected to receive data from a respective register. Moreover, since two quadrants share a row decoder, data is sequentially transferred from respective registers if the memory cell address for each quadrant are different. Thus, Lee fails to disclose or suggest writing data from a first and a second register into a single memory cell.

The Examiner now relies on Toda to teach this deficient feature. As to Toda, the Examiner references claim language recited in the "Summary of the Invention" at column 2, lines 35-42, which teaches that write-in registers 3 and 4 write to the memory cell array ML.

As to the motivation to combine, the Examiner states:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same word line for reading the first and second data and provide that the step of outputting data overlaps the step of reading data in Lee's EEPROM system because *this pipeline or parallel method would reduce the memory access time and speed up the data transfer, therefore, the whole system is enhanced and more efficient.*

The motivation statement mirrors the motivation statement corresponding to the obviousness rejection citing Otsuka and Egawa, discussed above, and does not address elements of claim 16, the claimed invention. Please note that in application of an obviousness rejection, the Examiner must provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references *to arrive at the claimed invention.* In this case, the Examiner has yet to address why it would have been obvious to modify Lee with a first register and a second register capable of writing to the same memory cell, so as to arrive at the claimed invention of claim 16. "[T]o use the same word line for reading the first and second data and provide that the

step of outputting data overlaps the step of reading data in Lee's EEPROM system," as stated by the Examiner, does not establish why one of ordinary skill in the art would have combined the reference to arrive at the claimed semiconductor structure, and steps, of claim 16. In this regard, the Examiner has failed to establish proper motivation to combine, and therefore, the obviousness rejection is improper.

For the foregoing reasons, the Examiner has failed to establish proper motivation to combine Lee and Toda to arrive at the claimed invention of claim 16. Claims 17, 22 and 21 are patentable at least based on dependency therefrom. Withdrawal of the rejection is respectfully solicited.

Conclusions

In light of the above remarks, this application should be considered in condition for allowance and passed to issue. If there are any questions regarding this response or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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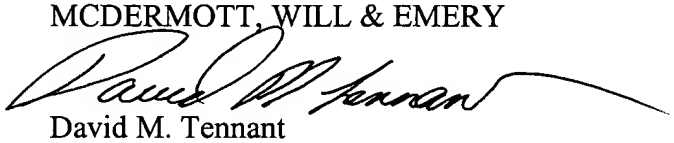

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